Application Note 0118

ezPyro - System Design Considerations for Low Noise and Optimum EMC Performance

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1 INTRODUCTION

The high level of integration within the ezPyro module (sensor, ADC, digital circuitry and power regulator) results in a device that is sensitive, robust and easy to integrate with the minimum of component count.

However, the system designer still has to consider how best to integrate the ezPyro into their design. This application note gives some guidelines as to how this might be achieved from the perspective of:

- Minimising system noise and its effect on the ezPyro
- EMC emissions from the circuit and associated system
- EMC immunity of the system to external interference

It is not possible to address all scenarios due to the wide variety of systems into which the ezPyro will be designed. However, general good practice guidelines are presented below to aid the designer in getting the best out of the ezPyro sensor.

2 SYSTEM NOISE

The datasheet bandwidth of the ezPyro sensor is in the range 1 to 200Hz. The biggest contributors to system level (also called “intra-system” or “platform”) noise in this frequency range are from power supplies and large capacitive load switching such as large digital circuits. These variations in the supply voltage or noise currents will be highly dependent on the other components in the system with every system being unique.

At these frequencies, interfering current will spread out in a conductor to use the path of least resistance. Therefore, the ezPyro can be best protected from in-band noise by correctly partitioning the design to keep noise sources further away and through careful use of a local ground plane.

3 DESIGN PARTITIONING

Good performance starts at the system design level. The principle behind design partitioning is to keep the interference source or “aggressor” away from the receiver or “victim”. In this instance, the ezPyro could be affected by noise from the power supply section of the system especially if it contains switching regulators. If a large or high speed digital circuit is employed then this can also generate significant noise at low frequencies. The I/O section of the system, where cables and interfaces connect to other components or systems, can also be subject to a variety of noise.

As shown in Figure 1, keeping the ezPyro as physically distant from the power supply and I/O zones should help reduce the effect of any system noise on the sensor.

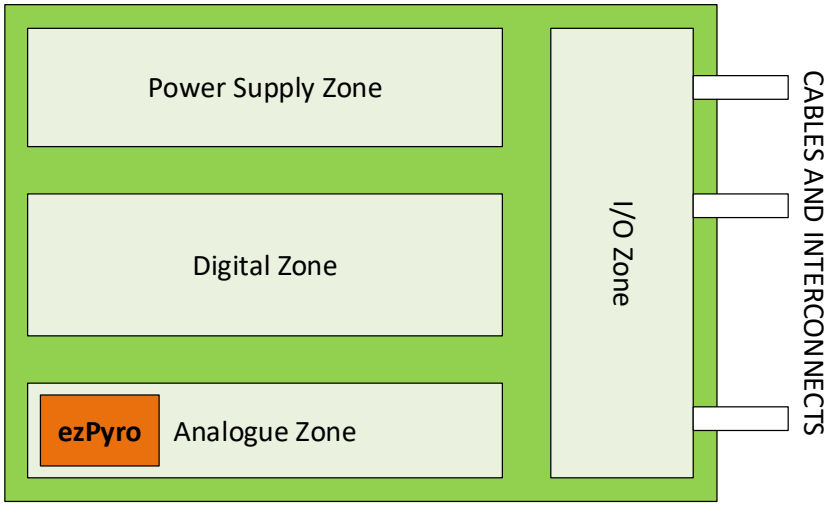

Figure 1 – Design partitioning for optimum performance

This method of partitioning applies equally to devices on a circuit board as it does to sub-assemblies within a discrete system. It is recognised that various design constraints placed on a system by factors outside of the designers control will result in a compromise from this ideal. Starting with good partitioning will result in increased performance and should be foremost in the designer’s mind.

4 POWER SUPPLY AND DECOUPLING

The ezPyro module contains an integrated Low Drop Out (LDO) linear regulator which provides high levels of power supply noise rejection at frequencies less than 1kHz. This aids integration into a wide range of systems with minimal additional component count.

Power supply stability is also aided by the correct use of decoupling capacitors which provide rejection of higher frequencies than the linear regulator can deal with. Performance of a decoupling system is dictated by several factors; the main ones are the value of capacitance and the impedance of the capacitor and interconnection at the frequencies of interest.

Two capacitors are required for the ezPyro. The first is the main power supply input capacitor from pin 1 to ground which decouples the 3V3 digital supply. The second is the internal voltage regulator output which requires a capacitor from pin 3 to ground (but with no other supply connections).

The recommended minimum value for both these decoupling capacitors is 100nF but if high levels of system noise are a concern then a 1uF (or larger) part could be used.

The HF impedance of the capacitor is dictated fundamentally by the package size where smaller parts have lower inductance i.e. a 0402 SMT part performs better at high frequencies (1MHz+) than a 1206 SMT part. The general recommendation would be to use 0402 size parts by default unless larger parts are in use elsewhere in the design that the designer wishes to re-use.

The high frequency impedance of the interconnect is a function of the inductance of the ezPyro > trace > capacitor > trace loop area. Optimum performance is achieved by keeping this loop area small by mounting the capacitor on the same side of the PCB as the ezPyro (if possible) and by placing the capacitor as close to the supply pins as PCB design rules allow.

5 PCB LAYOUT RECOMMENDATIONS

All good PCB design starts with planning a solid ground reference plane on one layer of the board. The benefits of this coherent ground plane are too numerous to go into in this application note but suffice to say it provides a low impedance, high frequency return path for signals that could cause EMC issues with the system.

In this instance there could be low frequency currents on this ground plane that may interfere with optimum sensor performance. As shown in Figure 2, it is recommended to isolate the sensor ground connections on layer 1 of the PCB only to form a local analogue ground plane. Connection of the analogue ground to the system ground plane can be made at the ground side of the main supply capacitor near pin 28 of the ezPyro but at no other point. No other traces should be routed underneath the device on Layer 1.

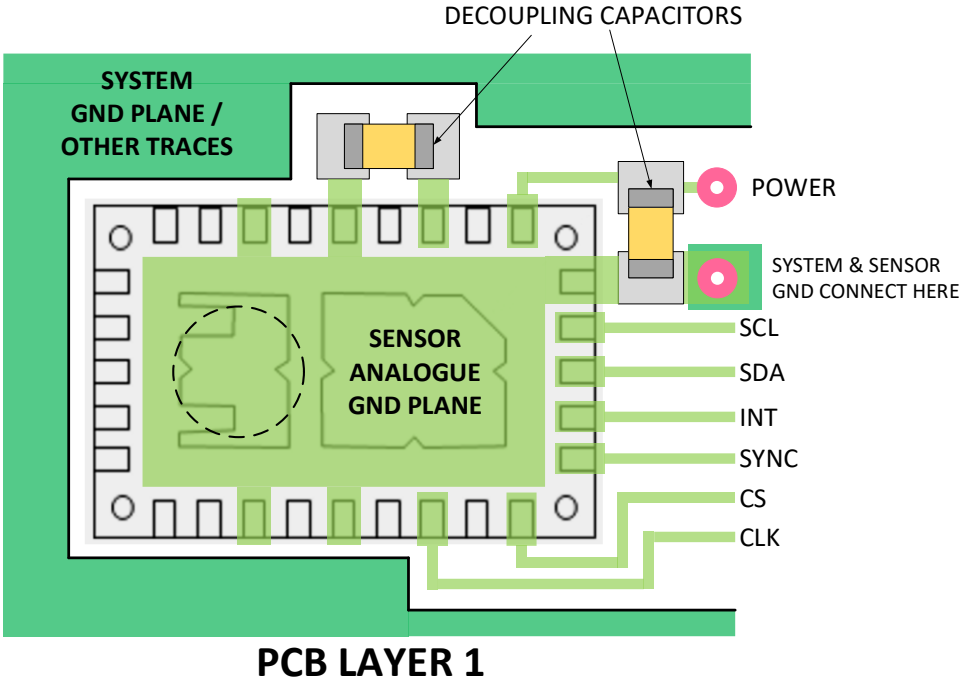

Figure 2 - Layer 1 PCB layout in the sensor area

The decoupling capacitors should also be placed as close to the device as practicable. In the event that they cannot be mounted on the same layer as the sensor then they should be placed as close as possible to the pins but on the opposite side of the PCB.

On the reverse side of the PCB, a solid ground plane is recommended, tied in to the analogue ground through a via as demonstrated in Figure 3. This ground plane should be extended underneath the digital traces all the way to the host to reduce the chances of EMC emissions or immunity problems resulting from these traces radiating of picking noise. If this is not possible then route a ground trace alongside the digital signals to keep the loop area of the signal return path small to improve signal integrity.

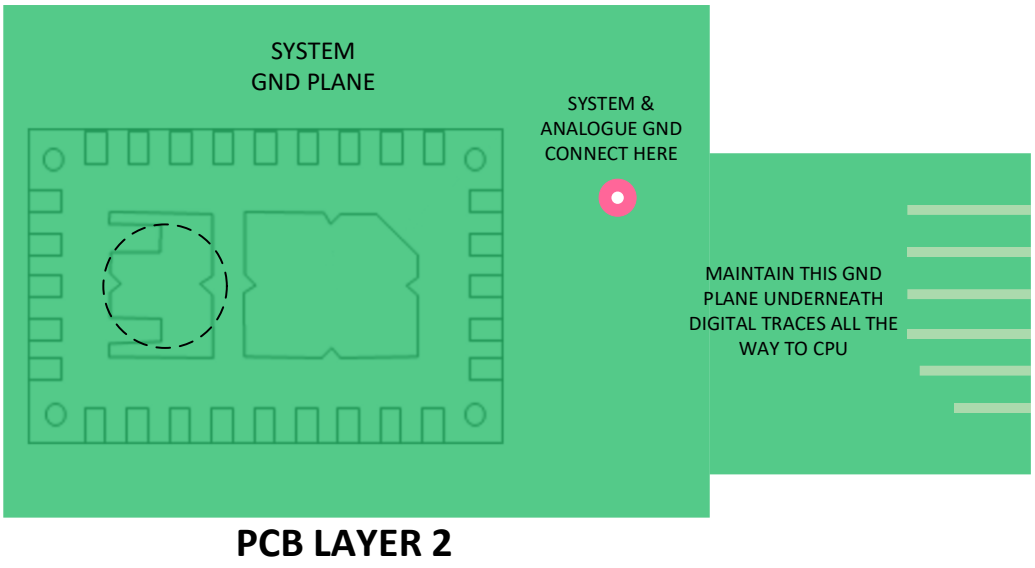

Figure 3 – Layer 2 PCB layout in the sensor area

6 SYSTEM DESIGN RECOMMENDATIONS

Following the design partitioning guidelines given above will aid the designer in achieving good performance.

One important consideration to be had is if the sensor is to be mounted on a remote PCB joined to the main CPU via a length of cable. The digital interface of the ezPyro removes the need for running sensitive analogue signals over a cable with the attendant problems that can cause. Nevertheless, the cable introduces an antenna-like element into the design which can pickup noise that can be detrimental to the ezPyro sensor.

in this case there are things the designer can do to stand the best possible chance of minimising system noise and EMC problems which are shown in figure 4.

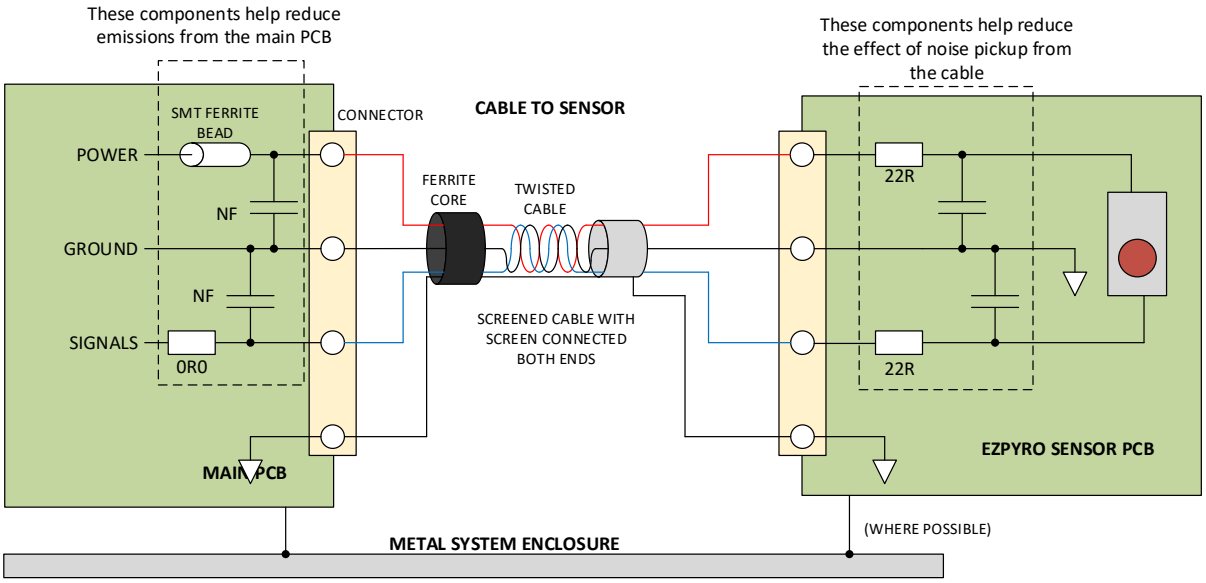

Figure 4 – Remote sensor noise mitigation measures

EMC radiated emissions caused by the ezPyro module will be minimal. With only low frequency digital signalling being employed the likelihood of problems being related to the module are minimal with good PCB layout.

However, unintentional digital noise from the main PCB can use the cable as a radiating antenna, causing radiated emissions problems. This can be mitigated by using RC low pass filters on the main PCB to attenuate the noise before it leaves the board. A ferrite bead is more appropriate in the power supply line to prevent voltage drops in the supply.

If this is not possible then noise can be supressed by the use of a HF ferrite core around the cable. These are readily available in a wide range of sizes and styles (round cable, ribbon cable, etc).

Emissions and noise immunity can often be improved by using a twisted cable or a shielded cable. If using a shielded cable, it is recommended to make provision for connecting the shield to the local ground at both ends.

Additionally, connecting the main PCB and the sensor PCB to any metal system enclosure may help with EMC noise immunity but care must be taken that it does not worsen system performance in other respects.

Routing of the cable should also be considered. Keeping the cable as short as practicable, routing it next to metal structures where possible, keeping it away from noise generating components such as power supplies and away from any apertures in a metal enclosure are all good practice.

If this cable exits a shielded enclosure then it is wise to make provision for terminating the shield of the cable at the point where it exits the metal shield.

The sensor has a small amount of ESD protection built in but not enough to withstand a direct strike from the test network used during EMC testing. It is recommended that the system be designed to prevent a charged-up user from making contact with the ezPyro sensor. This could be achieved through the use of physical distance – an 8kV air discharge will typically jump up to 5mm from a 4mm radius tip (depending heavily on geometry and

environmental conditions). Or it could be achieved by placing a transparent window between the sensor and user.

To reduce the effect of noise pickup from EMC immunity tests on the sensor, implementing an RC filter network on a remote sensor PCB is recommended. Good starting values are 22R and 100pF but can be varied to change performance.

7 CONCLUSION

Several methods of mitigating system noise for achieving the best performance of the ezPyro sensor have been presented for the use of the system designer.

Even if they are not used on the first design revision having the *option* to implement them can often save time during the development and testing cycle. Ultimately, some experimentation may be required in the host system to achieve the best compromise between performance and cost.