

Thin Film Pyroelectric Linear 255 Element Line Sensor Array

With Integrated Read-Out Electronics

Introduction

The Pyreos line sensor array utilises our unique thin-film pyroelectric PZT material to offer performance with unbeatable resolution, with the potential to capture all wavelengths of light and performance across a wide wavelength range. The ASIC readout electronics output is a multiplexed, amplified and filtered analogue signal for each sensor element. The sensor is housed in a low profile hermetic metal package along with a temperature sensor and is fitted with the customer's choice of filter window.



Product Features

Wavelength range	0.1 to 100 μm
Operating temperature	Un-cooled operation
Number of pixels	255 sensor elements
Pixel sizes	50 μm x 417.5 μm pixels in 2 lines of 128 pixels <i>NO spectral gaps – all wavelengths captured!</i> Vertical separation between lines: 45 μm In line pixel pitch: 100 μm
Pixel operability	96% with no more than 2 bad pixels in any 10
Dynamic range	>75 dB
Scan speed	10-1000 Hz

Applications

General IR spectroscopy	Portable, robust spectral engines
Lubricating oil monitoring	Quality, wear, adulteration,
Foodstuffs	Constitution, adulteration
Process monitoring	Wind turbine, petrochemical, pharmaceutical
Temperature measurement	Non-contact line scanning measurement
Imaging	Line scanning

Filters Available

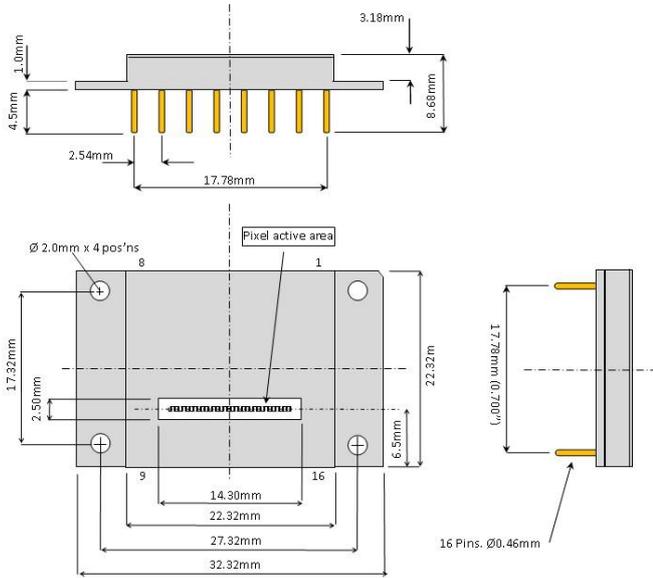
Part Number	PY0716
Filter Material	Silicon
Filter type	Broadband Antireflection coated Silicon

Order Information

Please quote PY-LA-S-255 and your desired customizations of this product. Contact: sales@pyreos.com

Please note: the information contained in this document is subject to change without further notification. Pyreos reserves the right to alter the performance and any resulting specification. Pyreos may choose not to supply any engineering sample devices as a commercial product. No responsibility is accepted for any consequential loss incurred. Pyreos Ltd, SMC, Alexander Crum Brown Road, Edinburgh EH9 3FF, UK. Tel: +441316507009, www.pyreos.com

Package Information



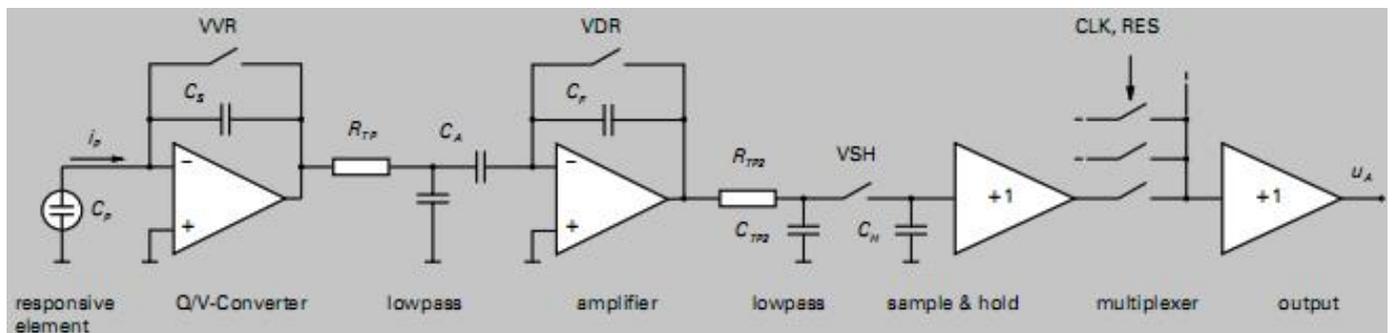
No.	Name	Comment
1.	CLK	Input clock CLK (trigger on rising edge)
2.	RES	Input clock RES (active low)
3.	VVR	Input clock VDR (active high)
4.	VDR	Input clock VDR (active high)
5.	VSH	Input clock VSH (active high)
6.	VD2	Operating voltage (+2.5 V)
7.	AVDD	Operating voltage (+5 V)
8.	VD2	Operating voltage (+2.5 V)
9.	OUT	Analogue signal output
10.	AGND	Ground
11.	n.c.	Not connected
12.	T+	Temperature sensor
13.	T-	Temperature sensor
14.	case	Case
15.	DGND	Ground
16.	DVDD	Operating voltage (+5 V)

Connect pin 6 to pin 8

Please remember to take ESD precautions when handling components

Circuit Diagram

The amplification circuit consists of low-noise preamplifiers for each individual sensor elements, analogue switches and an output amplifier. The pre-amplifiers transform the signal charges measured at each sensor element into a conditioned voltage. The amplified signal is then passed to sample and hold, multiplexer output buffer for the read-out process. The digital inputs are CMOS compatible. A 10k NTC thermistor is integrated within the package to monitor the line sensor temperature.



Thermistor is NTC, 1%. For more details check ERTJZEG103FA Datasheet on Industrial Panasonic website.

Please note: the information contained in this document is subject to change without further notification. Pyreos reserves the right to alter the performance and any resulting specification. Pyreos may choose not to supply any engineering sample devices as a commercial product. No responsibility is accepted for any consequential loss incurred. Pyreos Ltd, SMC, Alexander Crum Brown Road, Edinburgh EH9 3FF, UK. Tel: +441316507009, www.pyreos.com

Clock Parameters

Similar to all pyroelectric sensors, the Pyreos thin-film pyroelectric line sensor array responds to and detects a change in infrared radiation intensity. It therefore requires a pulsed source of infrared radiation for measurement purposes.

Parameter ¹	Relative Value	Min. Values	Recommended Value
Chopping Frequency ² f_{Ch}		10 Hz	128 Hz
Read-out Clock CLK $f_{CLK} = 2 * f_{Ch} * 268$	$1/t_{CLK}$	5.36 KHz	69 KHz
Reset clock low-impulse duration t_{RES}	$1/2 t_{CLK}$	1.8 μs	7.5 μs
Clock VVR high-impulse duration t_{VVR}	$2 t_{CLK}$	7.5 μs	30 μs
Clock VDR high-impulse duration t_{VDR}	$28 t_{CLK}$	200 μs	400 μs
Clock VSH high-impulse duration t_{VSH}	$1 t_{CLK}$	3.5 μs	15 μs

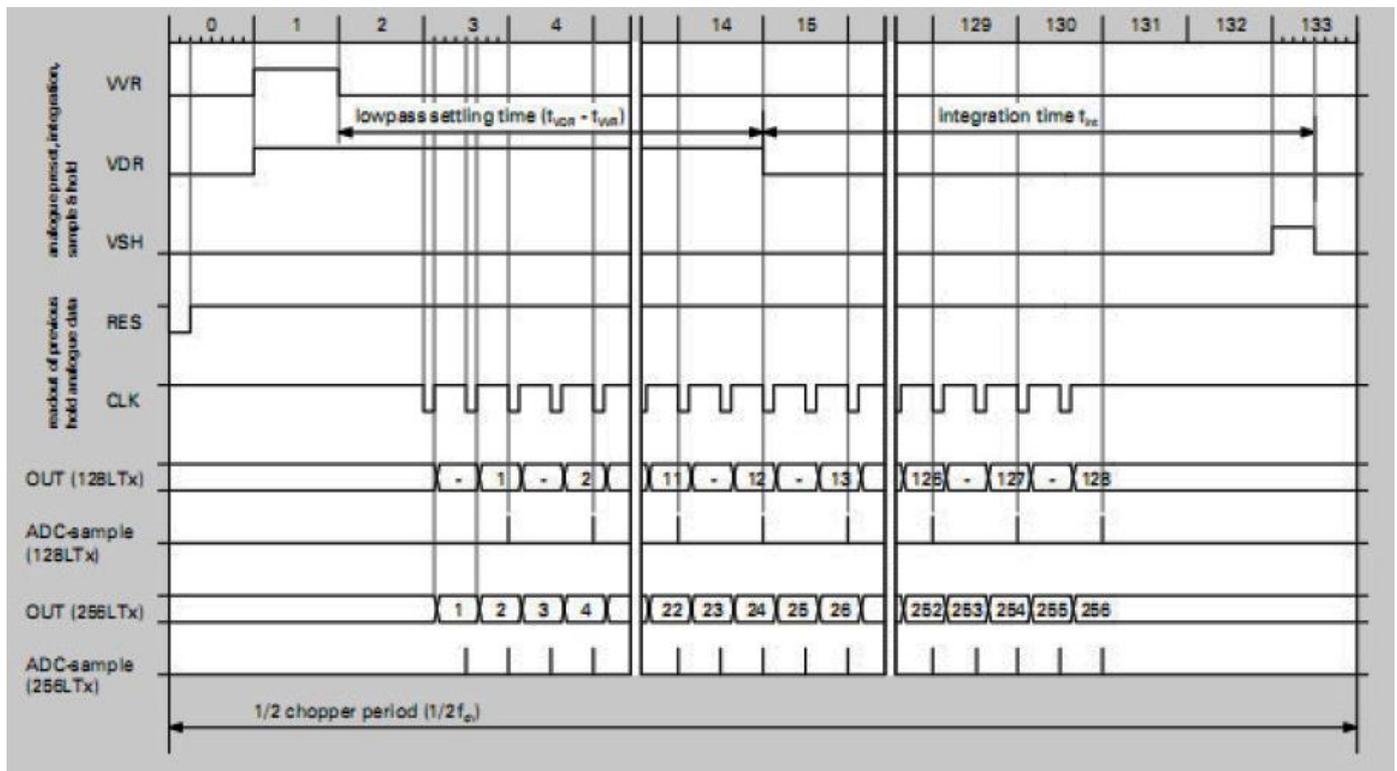
Maximum Settling Time at output t_{out} is 1 μ second

¹All values for VDD = 5 V, VD2 = 2.5V

² $t_{Ch low} = t_{Ch high}$

Clock Diagram

Pixel 1 is nearest pin 1 of the device.



Please note: the information contained in this document is subject to change without further notification. Pyreos reserves the right to alter the performance and any resulting specification. Pyreos may choose not to supply any engineering sample devices as a commercial product. No responsibility is accepted for any consequential loss incurred. Pyreos Ltd, SMC, Alexander Crum Brown Road, Edinburgh EH9 3FF, UK. Tel: +441316507009, www.pyreos.com