AN0129 Application Note: MCU Timing Control of ezPyro ASICs

1 INTRODUCTION

This application note covers the requirements for using a MCU to produce the signals for the ezPyro ASIC clock and sync signals. This allows synchronisation of the sampling with an IR source being controlled by that same MCU.

2 HOW TO OPERATE EZPYRO ASIC IN SLAVE MODE WITH EXTERNAL MCU AS TIMING MASTER

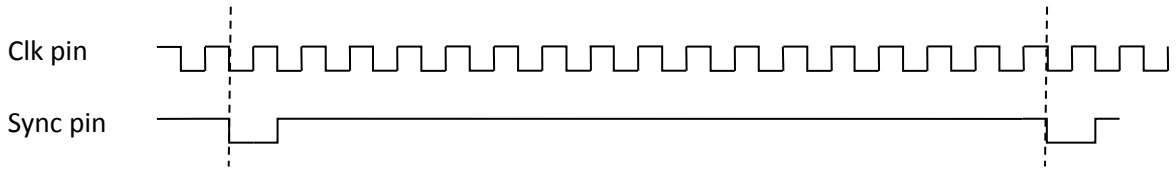

Figure 1: Relationship between Clk and Sync pin

For a system with a master ezPyro ASIC and follow by multiple slave ezPyro ASICs, the procedure is as follows:

- On the Master ezPyro ASIC, the SYNC register bit should be set to 0, CLK_OUT should be set to 1.
- On the Slave ezPyro ASIC, the SYNC register bit (bit 2 of Byte 1 in AFEP register) must be set to 1, and ignore the CLK_OUT register bit (bit 3 of Byte 1 in AFEP register).
- The Sync period is set by the byte 0 in the AFEP register of the Master ASIC. (note: byte 0 in the AFEP register of the Slave ASIC is also ignored).
- Connect the CLK and SYNC signal from the master to all the slave.

To simulate the behavioral of the master ezPyro ASIC by a microcontroller, these conditions should be met:

- The clock signal should be ~32kHz +/- 2.5% with a duty cycle between 45-55%
- The Sync signal (at Sync pin) will be active (low) for 1 clock period, starting at (or after) the falling clock edge (but must be high before the next rising clock edge).
- The Sync period (simulate the behavioral of byte 0 in the AFE register) should be: (value+1)*32 clock cycle. If a value 10 is desired, then the SYNC signal will be 351 clock periods high and 1 clock period low (SYNC period is:(10+1)*32=352).
- The data will be ready after the rising edge of the SYNC signal.

3 REVISION HISTORY

Revision Number	Revision Date	Description of Changes
1.0	30/11/2018	Initial document creation